Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**

**Diagram

Description automatically generated**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .007 X .005” min.**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: KW DIE SIZE .053 X .058” DATE: 2/7/23**

**MFG: SILICONIX THICKNESS: ” P/N: VP2410CHP**

**DG 10.1.2**

#### Rev B, 7/19/02